

2. Pin Information

2.1 Pin Assignments

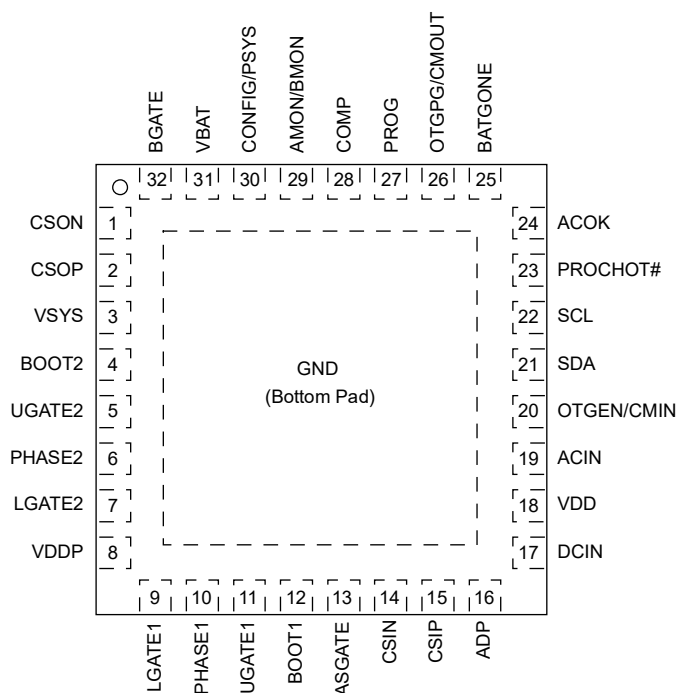


Figure 5. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
Bottom Pad	GND	Signal common to the IC. Unless otherwise stated, signals are referenced to the GND pin. GND should also be used as the thermal pad for heat dissipation.
1	CSON	Battery current sense negative input. Connect to the battery current resistor negative input. Place a ceramic capacitor between CSOP and CSON to provide differential mode filtering.
2	CSOP	Battery current sense positive input. Connect to the battery current resistor positive input. Place a ceramic capacitor between CSOP and CSON to provide differential mode filtering.
3	VSYS	Provides feedback voltage for MaxSystemVoltage regulation.
4	BOOT2	High-side MOSFET Q4 gate driver supply. Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT2 pins. Connect a 0.47μF bootstrap capacitor, which must have an effective capacitance higher than 0.25μF at 5V and x50 effective high-side MOSFET gate capacitance.
5	UGATE2	High-side MOSFET Q4 gate drive.
6	PHASE2	Current return path for the high-side MOSFET Q4 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q4 source, the low-side MOSFET Q3 drain, and one terminal of the inductor.
7	LGATE2	Low-side MOSFET Q3 gate drive.
8	VDDP	Power supply for the gate drivers. Connect to the VDD pin through a 4.7Ω resistor and connect a 2.2μF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4μF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

Pin Number	Pin Name	Description
9	LGATE1	Low-side MOSFET Q2 gate drive.
10	PHASE1	Current return path for the high-side MOSFET Q1 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q1 source, the low-side MOSFET Q2 drain, and one terminal of the inductor.
11	UGATE1	High-side MOSFET Q1 gate drive.
12	BOOT1	High-side MOSFET Q1 gate driver supply. Connect an MLCC capacitor across the BOOT1 and PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT1 pins. Connect a 0.47 μ F bootstrap capacitor, which must have an effective capacitance higher than 0.25 μ F at 5V and x50 effective high-side MOSFET gate capacitance.
13	ASGATE	Gate drive output to the P-channel adapter FET. The use of ASGATE FETs is optional. If they are not used, leave the ASGATE pin floating.
14	CSIN	Adapter current sense negative input.
15	CSIP	Adapter current sense positive input. The modulator also uses the CSIP pin for sensing input voltage in forward mode and output voltage in reverse mode.
16	ADP	Adapter input used to sense adapter voltage. ASGATE is turned on when the adapter voltage is higher than 3.2V. The ADP pin also provides one of the two internal low power LDO inputs.
17	DCIN	Internal LDO input that provides power to the IC. Connect a diode OR from the adapter and system outputs. Bypass DCIN with an MLCC capacitor. Connect a 10 Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connect a 4.7 μ F DCIN capacitor to GND. The capacitor must have an effective capacitance higher than 0.4 μ F at 30V.
18	VDD	Internal LDO output that provides the bias power for the internal analog and digital circuit. Connect a 2.2 μ F (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4 μ F at 5V and x1.6 effective capacitance at the BOOT pin at 5V. If VDD is pulled below 2V for more than 1ms, the RAA489118 resets all the SMBus register values to their defaults.
19	ACIN	Adapter voltage sense. Use a resistor divider externally to detect adapter voltage. The adapter voltage is valid if the ACIN pin voltage is greater than 0.6V.
20	OTGEN/ CMIN	Input pin. OTG function enable pin, stand-alone comparator input pin. When the OTG function is enabled and the general purpose comparator is disabled, pulling this pin high can activate the OTG function. When the general purpose comparator is enabled, this pin is the general purpose comparator input.
21	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification.
22	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification.
23	PROCHOT#	Open-drain output. Pulled low when ACHOT, DCHOT, or Low_VSYS are detected. IMVP compliant. Send an SMBus command to pull low with OTGCURRENT, BATGONE, ACOK, and the general purpose comparator (see Table 7).
24	ACOK	Adapter presence indicator output to indicate the adapter is ready.
25	BATGONE	Input pin to the IC. Logic high on this pin indicates the battery has been removed. Logic low on this pin indicates the battery is present. BATGONE pin logic high forces the BGATE FET to turn off in any circumstances.
26	OTGPG/ CMOUT	Open-drain output. OTG function output power-good indicator or the stand-alone comparator output. When the OTG function is enabled, this signal is low if the OTG output voltage is not within the regulation window. When the OTG function is not used, this signal is the general purpose comparator output. GP comparator must be disabled for OTGPG to function as expected.

Pin Number	Pin Name	Description
27	PROG	A resistor from the PROG pin to GND sets the following configurations: ▪ Default number of the battery cells in series: 2 to 7 cells ▪ Autonomous Charging mode: Enabled or disabled See Table 16 for programming options.
28	COMP	Error amplifier output. Connect a compensation network externally from COMP to GND.
29	AMON/ BMON	Adapter current, OTG output current, battery charging current, or battery discharging current monitor output. ▪ $V_{AMON} = 18x (V_{CSIP} - V_{CSIN})$ for adapter current monitor ▪ $V_{OTGCMON} = 18x (V_{CSIN} - V_{CSIP})$ for OTG output current monitor ▪ $V_{BMON_DISCHARGING} = 18x (V_{CSON} - V_{CSOP})$ for battery discharging current monitor ▪ $V_{BMON_CHARGING} = 36x (V_{CSOP} - V_{CSON})$ for battery charging current monitor
30	CONFIG/ PSYS	CONFIG/PSYS is tied to VDD for Buck-Boost charger configuration without BFET. CONFIG/PSYS is connected to the PSYS resistor for PSYS function for Buck-Boost charger configuration with BFET. Current source output that indicates the platform power consumption. PSYS gain = 0.236 μ A/W (default) or 0.118 μ A/W
31	VBAT	Battery voltage sensor. Used for trickle charging detection and Ideal Diode mode control. Connect an optional ceramic capacitor >1 μ F from VBAT to GND. The VBAT pin is also one of the two internal low power LDO inputs.
32	BGATE	Gate drive output to the P-channel FET connecting the system and the battery. This pin can go high to disconnect the battery, low to connect the battery, or operate in Linear mode to maintain the system voltage at the MinSystemVoltage level during trickle charging.