

6. Registers

The register descriptions below are based on current-sensing resistors $R_{s1} = 10\text{m}\Omega$ and $R_{s2} = 5\text{m}\Omega$, unless otherwise specified.

6.1 Register Summary

Table 1. Register Summary

Register Names	Register Address	Read/Write	Number of Bits	Description	Default
ChargeCurrentLimit	0x14	R/W	11	[12:2], LSB size 8mA	256mA: CONFIG = VDD 0A: Otherwise
MaxSystemVoltage	0x15	R/W	12	[14:3], LSB size 16mV	8.4V 12.608V 16.8V 21.008V 25.2V 29.408V (Set by PROG pin)
Control7	0x36	R/W	3	[7], [1:0], configures various charger options	0x0000
Control6	0x37	R/W	8	[7:0], configures various charger options	0x0040 or 0x0043 ^[1]
Control5	0x38	R/W	16	Configures various charger options	0x0000
Control0	0x39	R/W	16	Configures various charger options	0x0000
Information1	0x3A	R	16	Indicates various charger statuses	0x0000
AdapterCurrentLimit2	0x3B	R/W	11	[12:2], LSB size 8mA	1.504A
Control1	0x3C	R/W	16	Configures various charger options	0x0200
Control2	0x3D	R/W	16	Configures various charger options	0x0000
MinSystemVoltage	0x3E	R/W	8	[13:6], LSB size 128mV	5.12V 7.68V 10.24V 12.80V 15.36V 17.92V (Set by PROG pin)
AdapterCurrentLimit1	0x3F	R/W	11	[12:2], LSB size 8mA	0.48A or 1.504A (Set by PROG pin)
Revision ID	0x44	R	8	Revision ID register - Read only	0x00
ACProchot#	0x47	R/W	6	[12:7] Adapter current PROCHOT# threshold, 256mA resolution for $10\text{m}\Omega R_{s1}$.	3.072A
DCProchot#	0x48	R/W	6	[13:8] Battery discharging current PROCHOT# threshold, 512mA resolution for $5\text{m}\Omega R_{s2}$.	4.096A
OTG Voltage	0x49	R/W	12	[14:3], LSB size 18mV, OTG mode voltage reference	5.004V
OTG Current	0x4A	R/W	9	[12:4], LSB size 32mA, OTG mode maximum current limit	0.512A

Table 1. Register Summary (Cont.)

Register Names	Register Address	Read/Write	Number of Bits	Description	Default
V _{IN} Voltage	0x4B	R/W	6	[13:8], LSB size 512mV, V _{IN} loop voltage reference	4.096V
Control3	0x4C	R/W	16	Configures various charger options	0x0000 or 0x0080 ^[2]
Information2	0x4D	R	16	Indicates various charger statuses	0x0000
Control4	0x4E	R/W	16	Configures various charger options	0x0000
Information3	0x90	R	1	[1] indicates pass-through mode status	0x0000
Manufacturer ID	0xFE	R	8	Manufacturer ID register – 0x49 - Read only	0x0049
Device ID	0xFF	R	8	Device ID register - Read only	0x0018

1. The default value for the VSYS UV field depends on the CONFIG pin state and whether powering up from battery.
2. Control3 Bit[7] is set by PROG pin, see [Table 16](#).

6.2 DAC Register Summary

Table 2. DAC Summary Table^[1]

ADDR Bit	Charge Current Limit (R _{s2} = 5mΩ)		Max System Voltage	Min System Voltage	Adapter Current Limit1 (R _{s1} = 10mΩ)	Adapter Current Limit2 (R _{s1} = 10mΩ)	V _{IN} Voltage (ADP Min Voltage or BAT Min Voltage)	ACProchot# (ACHOT) (R _{s1} = 10mΩ)	DCProchot# (DCHOT) (R _{s2} = 5mΩ)	OTG Voltage	OTG Current (R _{s1} = 10mΩ)
	0x14		0x15	0x3E	0x3F	0x3B	0x4B	0x47	0x48	0x49	0x4A
[0]	-		-	-	-	-	-	-	-	-	-
[1]	-		-	-	-	-	-	-	-	-	-
[2]	8mA		-	-	8mA	8mA	-	-	-	-	-
[3]	16mA		16mV	-	16mA	16mA	-	-	-	18mV	-
[4]	32mA		32mV	-	32mA	32mA	-	-	-	36mV	32mA
[5]	64mA		64mV	-	64mA	64mA	-	-	-	72mV	64mA
[6]	128mA		128mV	128mV	128mA	128mA	-	-	-	144mV	128mA
[7]	256mA		256mV	256mV	256mA	256mA	-	256mA	-	288mV	256mA
[8]	512mA		512mV	512mV	512mA	512mA	512mV	512mA	512mA	576mV	512mA
[9]	1024mA		1024mV	1024mV	1024mA	1024mA	1024mV	1024mA	1024mA	1152mV	1024mA
[10]	2048mA		2048mV	2048mV	2048mA	2048mA	2048mV	2048mA	2048mA	2304mV	2048mA
[11]	4096mA		4096mV	4096mV	4096mA	4096mA	4096mV	4096mA	4096mA	4608mV	4096mA
[12]	8192mA		8192mV	8192mV	8192mA	8192mA	8192mV	8192mA	8192mA	9216mV	8192mA
[13]	-		16384mV	16384mV	-	-	16384mV	-	16384mA	18432mV	-
[14]	-		0mV	-	-	-	-	-	-	0mV	-
[15]	-		-	-	-	-	-	-	-	-	-
Max	12.16A (0x17C0)		32.256V (0x3F00)	25.088V (0x3100)	12.16A (0x17C0)	12.16A (0x17C0)	27.648A (0x3600)	12.8A (0x1900)	25.6A (0x3200)	32.256V (0x3800)	8.192A (0x1000)
Default	CFG = VDD	CFG ≠ VDD	Set by PROG	Set by PROG	0.48A (0x00F0) or 1.504A (0x02F0) (Set by PROG)	1.504A (0x02F0)	4.096V (0x0800)	3.072A (0x0600)	4.096A (0x0800)	5.004V (0x08B0)	0.512A (0x0100)
	0.256A (0x0080)	0A (0x0000)									

1. Each of the DAC registers accepts any value, but only the valid register bits are written to the register and the voltage or current value is clamped at the indicated maximum. The RAA489118 accepts a 0V command for the MaxSystemVoltage register, but the register value does not change. The MinSystemVoltage value should be lower than the MaxSystemVoltage value.

6.3 Control Registers

The Control registers configure the operation of the RAA489118. To change the configuration after a POR, write to the appropriate control registers using the Write-word protocol shown in [Figure 37](#).

Table 3. Control0 Register 0x39H

Bit	Bit Name	Description
[15:13]	Forward Buck Phase Comparator Threshold Offset	Bit[15:13] adjusts the phase comparator threshold offset for the forward buck mode. 000 = 0mV (default) 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
[12:10]	Forward Buck-boost, Forward Boost, and Reverse Boost Phase Comparator Threshold Offset	Bit[12:10] adjusts the phase comparator threshold offset for the forward buck-boost, forward boost, and reverse boost modes. 000 = 0mV (default) 001 = 0.5mV 010 = 1mV 011 = 1.5mV 100 = -2mV 101 = -1.5mV 110 = -1mV 111 = -0.5mV
[9,8,0]	Reverse Buck and Reverse Buck-boost Phase Comparator Threshold Offset	Bit[9,8,0] adjusts the phase comparator threshold offset for the reverse buck and reverse buck-boost modes. 000 = 0mV (default) 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
[7]	SMBus Timeout	Bit[7] enables or disables the charger timeout function in NVDC charging mode (CONFIG pulled low). If the adapter is present and the RAA489118 does not receive a write command to the MaxSystemVoltage(0x15) or ChargeCurrentLimit(0x14) register within the time set by Control3 register Bit[12:11], RAA489118 terminates charging. After the timeout occurs, writing the MaxSystemVoltage(0x15) or ChargeCurrentLimit(0x14) register re-enables charging. 0 = Enable the SMBus timeout function (default) 1 = Disable the SMBus timeout function For battery-charging only mode (CONFIG tied to VDD), this bit is irrelevant and the SMBus Timeout feature is always disabled.
[6:5]	High-Side FET Short Detection Threshold	Bit[6:5] configures the high-side FET short detection phase node voltage threshold while the low-side FET turns on. 00 = 800mV (default) 01 = 500mV 10 = 600mV 11 = 400mV

Table 3. Control0 Register 0x39H (Cont.)

Bit	Bit Name	Description																																													
[4:3]	DCProchot# Threshold in Battery Only Low Power Mode	Control7[1] and Control0[4:3] configure the battery discharging current DCProchot# threshold in battery only Low Power mode as indicated by Information1 register 0x3A Bit[15]. If PSYS is enabled, the battery discharge current DCProchot# threshold is instead set by the DCProchot# register 0x48 setting.																																													
		<table><tr><th>Control7[1]</th><th>Control0[4:3]</th><th>R_{s2} = 20mΩ (A)</th><th>R_{s2} = 10mΩ (A)</th><th>R_{s2} = 5mΩ (A)</th></tr><tr><td>0 (default)</td><td>00 (default)</td><td>6</td><td>12</td><td>24</td></tr><tr><td>0</td><td>01</td><td>5</td><td>10</td><td>20</td></tr><tr><td>0</td><td>10</td><td>4</td><td>8</td><td>16</td></tr><tr><td>0</td><td>11</td><td>3</td><td>6</td><td>12</td></tr><tr><td>1</td><td>00</td><td>2.5</td><td>5</td><td>10</td></tr><tr><td>1</td><td>01</td><td>2</td><td>4</td><td>8</td></tr><tr><td>1</td><td>10</td><td>1.5</td><td>3</td><td>6</td></tr><tr><td>1</td><td>11</td><td>1</td><td>2</td><td>4</td></tr></table>	Control7[1]	Control0[4:3]	R _{s2} = 20mΩ (A)	R _{s2} = 10mΩ (A)	R _{s2} = 5mΩ (A)	0 (default)	00 (default)	6	12	24	0	01	5	10	20	0	10	4	8	16	0	11	3	6	12	1	00	2.5	5	10	1	01	2	4	8	1	10	1.5	3	6	1	11	1	2	4
		Control7[1]	Control0[4:3]	R _{s2} = 20mΩ (A)	R _{s2} = 10mΩ (A)	R _{s2} = 5mΩ (A)																																									
		0 (default)	00 (default)	6	12	24																																									
		0	01	5	10	20																																									
		0	10	4	8	16																																									
		0	11	3	6	12																																									
		1	00	2.5	5	10																																									
		1	01	2	4	8																																									
		1	10	1.5	3	6																																									
		1	11	1	2	4																																									
[2]	Input Voltage Regulation Loop	Bit[2] enables or disables the input voltage regulation loop. 0 = Enable the input voltage regulation loop (default) 1 = Disable the input voltage regulation loop																																													
[1]	Force Buck Mode	Bit[1] disables or enables Force Buck mode. If the Force Buck mode bit is enabled, the Buck-Boost window narrows. 0 = Disable Force Buck mode (default) 1 = Enable Force Buck mode																																													

Table 4. Control1 Register 0x3CH

Bit	Bit Name	Description
[15:14]	General Purpose Comparator Assertion Debounce Time	Bit[15:14] configures the general purpose comparator assertion debounce time. 00 = 2 μ s (default) 01 = 12 μ s 10 = 2ms 11 = 5s
[13]	Exit Learn Mode Option	Bit[13] provides the option to Exit Learn mode when the battery voltage is lower than the MinSystemVoltage register setting. 0 = Stay in Learn mode even if $V_{BAT} < \text{MinSystemVoltage}$ register setting (default) 1 = Exit Learn mode if $V_{BAT} < \text{MinSystemVoltage}$ register setting
[12]	Learn Mode	Bit[12] enables or disables Battery Learn mode. 0 = Disable Battery Learn mode (default) 1 = Enable Battery Learn mode To enter Learn mode, the BATGONE pin must be low, that is, the battery must be present. Renesas recommends to disable the slew rate control (Control6 Bit[6] = 0) when using Learn mode.
[11]	OTG Function	Bit[11] enables or disables the OTG function. 0 = Disable the OTG function (default) 1 = Enable the OTG function

Table 4. Control1 Register 0x3CH (Cont.)

Bit	Bit Name	Description
[10]	Audio Filter	Bit[10] enables or disables the audio filter function. 0 = Disable the audio filter function (default) 1 = Enable the audio filter function
[9:8]	Switching Frequency	Bit[9:8] configures the switching frequency. 00 = 1MHz 01 = 839kHz 10 = 732kHz (default) 11 = 635kHz
[7]	Not Used	Not used
[6]	Turbo	Bit[6] enables or disables Turbo mode. When the turbo function is enabled, the BGATE FET turns on in Turbo mode. See Table 15 for the BGATE ON/OFF truth table. 0 = Enable Turbo mode (default) 1 = Disable Turbo mode
[5]	AMON/BMON Function	Bit[5] enables or disables the current monitor function AMON and BMON. 0 = Enable AMON/BMON (default) 1 = Disable AMON/BMON Bit[5] is only valid in Battery Only mode. When the adapter is present, AMON/BMON is automatically enabled and Bit[5] becomes invalid.
[4]	AMON or BMON	Bit[4] selects AMON or BMON as the AMON/BMON pin output. 0 = AMON (default) 1 = BMON
[3]	PSYS	Bit[3] enables or disables the system power monitor PSYS function. 0 = Disables the PSYS function (default) 1 = Enables the PSYS function
[2]	VSYS	Bit[2] enables or disables the buck-boost charger switching VSYS output. When disabled, the RAA489118 stops switching and forces the BGATE FET on. 0 = Enables VSYS output (default) 1 = Disables VSYS output
[1:0]	Low_VSYS_Prochot# Reference	Bit[1:0] configures the Low_VSYS_Prochot# assertion. 00 = 6.0V (default) 01 = 6.3V 10 = 6.6V 11 = 6.9V

Table 5. Control2 Register 0x3DH

Bit	Bit Name	Description															
[15:14]	Trickle Charging Current	Bit[15:14] configures the charging current in Trickle Charging mode. 00 = 512mA (default) 01 = 256mA 10 = 128mA 11 = 1024mA															
[13]	OTG Function Enable Debounce Time	Control2 Bit[13] and Control 3 Bit[0] configures the OTG function debounce time from when the RAA489118 receives the OTG enable command. <table border="1"> <thead> <tr> <th>Control2[13]</th><th>Control3[0]</th><th>OTG Start-Up Delay</th></tr> </thead> <tbody> <tr> <td>0 (default)</td><td>0 (default)</td><td>1.3s</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td>150ms</td></tr> <tr> <td>1</td><td>1</td><td>7.5ms</td></tr> </tbody> </table>	Control2[13]	Control3[0]	OTG Start-Up Delay	0 (default)	0 (default)	1.3s	0	1		1	0	150ms	1	1	7.5ms
Control2[13]	Control3[0]	OTG Start-Up Delay															
0 (default)	0 (default)	1.3s															
0	1																
1	0	150ms															
1	1	7.5ms															
[12]	Two-Level Adapter Current Limit Function	Bit[12] enables or disables the two-level adapter current limit function. 0 = Disables the two-level current limit function (default) 1 = Enables the two-level current limit function															
[11]	Adapter Insertion to Switching Debounce	Bit[11] configures the debounce time from adapter insertion to when ACOK is asserted high. 0 = 1.3s (default) 1 = 150ms After VDD POR, for the first time the adapter is plugged in, the ASGATE turn-on delay is always 150ms, regardless of the Bit[11] setting. This bit sets the ASGATE turn-on delay only after ASGATE turns off at least one time when VDD is above its POR value and the Bit[11] default is 0 for 1.3s.															
[10:9]	Prochot# Debounce	Bit[10:9] configures the PROCHOT# debounce time before its assertion for ACProchot# and DCProchot#. The Low_VSYS_Prochot# has a fixed 8μs debounce time. 00: 7μs (default) 01: 100μs 10: 500μs 11: 1ms															
[8:6]	Prochot# Duration	Bit[8:6] configures the minimum duration of the PROCHOT# signal when asserted. 000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 500μs 110 = 100μs 111 = 0s															
[5]	ASGATE in OTG Mode	Bit[5] turns the ASGATE FET on or off in OTG mode. 0 = Turn on ASGATE in OTG mode (default) 1 = Turn off ASGATE in OTG mode															

Table 5. Control2 Register 0x3DH (Cont.)

Bit	Bit Name	Description
[4]	CMIN Reference	Bit[4] configures the general purpose comparator reference voltage when an adapter is attached. (In Battery-Only low-power mode, the reference voltage is 1.2V regardless of this bit.) 0 = 1.2V (default) 1 = 2V
[3]	General Purpose Comparator	Bit[3] enables or disables the general purpose comparator. 0 = Enable the general purpose comparator (default) 1 = Disable the general purpose comparator
[2]	CMOUT Polarity	Bit[2] configures the general purpose comparator output polarity when asserted. The comparator reference voltage is connected at the inverting input node. 0 = CMOUT is High when CMIN is higher than reference (default) 1 = CMOUT is Low when CMIN is higher than reference
[1:0]	Pass-Through Mode	Bit[1:0] configures the Pass-Through Mode (PTM). 00 = Disable normal PTM and forced PTM (default) 01 = Enable normal PTM 10 = Not Used 11 = Enable Forced PTM

Table 6. Control3 Register 0x4CH

Bit	Bit Name	Description ⁷
[15]	Reread PROG Pin Resistor	Bit[15] specifies whether to reread the PROG pin resistor. 0 = Reread PROG pin resistor (default) 1 = Do not reread PROG pin resistor
[14]	Reload ACLIM When Adapter Is Plugged In	Bit[14] specifies whether to reload the AdapterCurrentLimit1 register set by the PROG pin resistor. 0 = Reload the AdapterCurrentLimit1 register (default) 1 = Do not reload the AdapterCurrentLimit1 register
[13]	Autonomous Charging Termination Time	Bit[13] configures the autonomous charging termination time. 0 = 20ms (default) 1 = 200ms
[12:11]	Charger Timeout	Bit[12:11] configures the SMBus charger timeout time. 00 = 175s (default) 01 = 87.5s 10 = 43.75s 11 = 5s
[10]	BGATE Force OFF	Bit[10] configures the BGATE operation between normal and force off. 0 = Normal BGATE operation (default) 1 = Force BGATE MOSFET off
[9]	PSYS Gain	Bit[9] configures the system power monitor PSYS output gain. 0 = 0.236 μ A/W (default) 1 = 0.118 μ A/W

Table 6. Control3 Register 0x4CH (Cont.)

Bit	Bit Name	Description7															
[8]	Exit IDM Timer	Control7[7] and Control3[8] configure the Ideal Diode mode exit timer when the battery discharge current is less than 380mA.															
		<table><tr><th>Control3 [8]</th><th>Control7 [7]</th><th>IDM Timer</th></tr><tr><td>0 (default)</td><td>0 (default)</td><td>40ms</td></tr><tr><td>0</td><td>1</td><td>5ms</td></tr><tr><td>1</td><td>0</td><td>80ms</td></tr><tr><td>1</td><td>1</td><td>1ms</td></tr></table>	Control3 [8]	Control7 [7]	IDM Timer	0 (default)	0 (default)	40ms	0	1	5ms	1	0	80ms	1	1	1ms
		Control3 [8]	Control7 [7]	IDM Timer													
		0 (default)	0 (default)	40ms													
		0	1	5ms													
		1	0	80ms													
1	1	1ms															
[7]	Charging Mode	Bit[7] selects the charging mode. 0 = Enable Autonomous Charging mode 1 = Battery charging current control through SMBus Default is determined by PROG and CONFIG.															
[6]	AC and CC Feedback Gain	Bit[6] configures AC and CC feedback gain for high current. 0 = x1 (default) 1 = x0.5															
[5]	Adapter-Side Current Limit Loop	Bit[5] enables or disables the adapter-side input current limit loops for forward and reverse/OTG modes. 0 = Enable adapter-side current limit loops (default) 1 = Disable adapter-side current limit loops															
[4]	Adapter-Side Current Limit Loop when BATGONE = 1	Bit[4] enables or disables the adapter-side current limit loop, in forward mode, when BATGONE = 1. 0 = Enable adapter-side current limit loop when BATGONE = 1 (default) 1 = Disable adapter-side current limit loop when BATGONE = 1															
[3]	AMON/BMON Direction	Bit[3] configures the AMON/BMON direction. 0 = Adapter current monitor/battery charging current monitor (default) 1 = OTG output current monitor/battery discharging current monitor															
[2]	Digital Reset	Bit[2] resets all SMBus register values to the POR default value. 0 = Idle (default) 1 = Reset															
[1]	Buck-Boost Stretch CCM Period	Control3 Bit[1] and Control4 Bit[8] configure the Buck-Boost stretch CCM period (T2 TIME).															
		<table><tr><th>Control3[1]</th><th>Control4[8]</th><th>T2 Time</th></tr><tr><td>0</td><td>0</td><td>0.6x (default)</td></tr><tr><td>0</td><td>1</td><td>1x</td></tr><tr><td>1</td><td>0</td><td>3x</td></tr><tr><td>1</td><td>1</td><td>2x</td></tr></table>	Control3[1]	Control4[8]	T2 Time	0	0	0.6x (default)	0	1	1x	1	0	3x	1	1	2x
		Control3[1]	Control4[8]	T2 Time													
		0	0	0.6x (default)													
		0	1	1x													
		1	0	3x													
1	1	2x															
[0]	OTG Start-Up Delay	Refer to the description of Control2[13] in Table 5 .															

Table 7. Control4 Register 0x4EH

Bit	Bit Name	Description
[15:14]	Dither Enable	Bit[15:14] disables or selects the switching frequency dithering function. 00 = Disable dither (default) 01 = Dither 100 - 102% 10 = Dither 100 - 104% 11 = Dither 100 - 106%
[13]	ADP Discharge	Bit[13] enables or disables the ADP discharge function. Typical 10mA. 0 = Disable ADP discharge function (default) 1 = Enable ADP discharge function
[12]	VSYS Sink	Bit[12] enables or disables the VSYS discharge function. Typical 10mA. 0 = Disable VSYS discharge function (default) 1 = Enable VSYS discharge function
[11]	BGATE Tri-state	Bit[11] enables or disables the BGATE tri-state function. 0 = Disable BGATE tri-state (default) 1 = Enable BGATE tri-state
[10]	Buck-Boost Min T3 Time	Bit[10] selects the minimum T3 time when in the buck-boost mode. 0 = Long (default) 1 = Short
[9]	Buck-Boost T2 time in DCM	Bit[9] selects the buck-boost T2 time in the discontinuous-conduction mode (DCM). 0 = Reduced T2 time (increases switching frequency in DCM) (default) 1 = Normal T2 time
[8]	Buck-Boost Stretch CCM Period	Refer to the description of Control3 Bit[1] in Table 6 .
[7]	OTGCURRENT PROCHOT#	Bit[7] enables or disables PROCHOT# trigger with OTGCURRENT. 0 = Disable PROCHOT# trigger with OTGCURRENT (default) 1 = Enable PROCHOT# trigger with OTGCURRENT
[6]	BATGONE PROCHOT#	Bit[6] enables or disables PROCHOT# trigger with BATGONE. 0 = Disable PROCHOT# trigger with BATGONE (default) 1 = Enable PROCHOT# trigger with BATGONE
[5]	ACOK PROCHOT#	Bit[5] enables or disables PROCHOT# trigger with ACOK. 0 = Disable PROCHOT# trigger with ACOK (default) 1 = Enable PROCHOT# trigger with ACOK
[4]	Comparator PROCHOT#	Bit[4] enables or disables PROCHOT# trigger with General Purpose Comparator rising. 0 = Disable PROCHOT# trigger with General Purpose Comparator rising (default) 1 = Enable PROCHOT# trigger with General Purpose Comparator rising
[3:2]	ACOK falling or BATGONE Rising Debounce	Bit[3:2] configures the debounce time from ACOK falling or BATGONE rising to PROCHOT# trip. 00 = 2μs (default) 01 = 25μs 10 = 125μs 11 = 250μs

Table 7. Control4 Register 0x4EH (Cont.)

Bit	Bit Name	Description
[1]	PROCHOT# Clear	Bit[1] clears PROCHOT#. 0 = Idle (default) 1 = Clear PROCHOT#
[0]	PROCHOT# Latch	Bit[0] manually resets PROCHOT#. 0 = PROCHOT# signal auto-clear (default) 1 = Latch PROCHOT# low when tripped

Table 8. Control5 Register 0x38H

Bit	Bit Name	Descriptions
[15:14]	Internal Compensation Resistance	Bit[15:14] set the internal compensation resistance 00 = 1.26 K Ω (default) 01 = 773 Ω 10 = 3.6 K Ω 11 = 1.88 K Ω
[13]	Force BGATE On	Bit[13] enables or disables the Force BGATE On function 0 = Normal BGATE operation (default) 1 = Force BGATE On
[12]	Unused	-
[11]	VBAT Regulation Loop in OTG Mode	Bit[11] enables or disables the VBAT (VIN) voltage regulation during OTG (reverse) mode 0 = Disable (default) 1 = Enable
[10:8]	Two-Level ACLIM T2 Time	Bit[10:8] sets the T2 time corresponding to AdapterCurrentLimit2 when two-level adapter current limit function is enabled. 000 = 10 μ s (default) 001 = 100 μ s 010 = 500 μ s 011 = 1ms 100 = 300 μ s 101 = 750 μ s 110 = 2ms 111 = 10ms
[7]	VSYSOK 0.6V Comparator	Bit[7] enables or disables the 0.6V comparator. 0 = Enable (default) 1 = Disable
[6]	VSYSOK 10mA Current Source	Bit[6] enables or disables the 10mA current source. 0 = Enable (default) 1 = Disable
[5]	OTGPG/CMOUT Selection	Bit[5] selects the signal routed to the OTGPG/CMOUT pin. 0 = OTGPG (default) 1 = CMOUT
[4]	VSYSOV/OTGOV Control	Bit[4] enables or disables VSYS and OTG overvoltage protections. 0 = Enable (default) 1 = Disable

Table 8. Control5 Register 0x38H

Bit	Bit Name	Descriptions
[3]	Unused	-
[2:0]	Two-Level ACLIM T1 Time	Bit[2:0] sets the T1 time corresponding to AdapterCurrentLimit1 when two-level adapter current limit function is enabled. 000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 0.5ms 110 = 0.1ms 111 = 0ms

Table 9. Control6 Register 0x37H

Bit	Bit Name	Description
[15:8]	Not Used	Not used
[7]	Turn off BGATE at VSYSOV	Bit[7] configures the BGATE behavior during VSYS overvoltage. 0 = No action (default) 1 = Turn off BGATE
[6]	Slew Rate Control for Charge Current, Maximum System Voltage, and OTG Voltage	Bit[6] enables or disables the slew rate control for charger current, maximum system voltage, and OTG voltage. 0 = Disable the slew rate control 1 = Enable the slew rate control (default) Slew is limited to 1 DAC LSB per 16 clock cycles (1μs each). Nominal slew rates: 1mV/μs for system voltage, 0.5mA/μs for charging current with $R_{s2} = 5m\Omega$, and 1.125mV/μs for OTG voltage.
[5]	OTG Undervoltage Protection	Bit[5] enables or disables the OTG undervoltage protection 0 = Enable OTG undervoltage protection (default) 1 = Disable OTG undervoltage protection
[4]	Clear CMOUT Latch Data	Bit[4] clears the current CMOUT data when written to 1. The CMOUT latch data can be read from Bit[4] when Control6[3] = 0 (CMOUT Latch is enabled). 0 = Do not clear CMOUT latch data (default) 1 = Clear CMOUT latch data
[3]	CMOUT Latch	Bit[3] enables or disables the CMOUT latch function. 0 = Enable the CMOUT latch function (default) 1 = Disable the CMOUT latch function
[2:0]	VSYS Undervoltage Threshold	Bit[2:0] set VSYS under voltage threshold. 000 = Disable (default when CONFIG = VDD or when inserting the battery for the first time) 001 = 3.0V 010 = 3.9V 011 = 4.8V (default when CONFIG pulled low, except after inserting battery for the first time) 100 = 5.7V 101 = 6.6V 110 = 7.5V 111 = 8.4V

Table 10. Control7 Register 0x36H

Bit	Bit Name	Description															
[15:8]	Not Used	Not Used															
[7]	Exit IDM Timer	Control7[7] and Control3[8] configure the Ideal Diode mode exit timer when the battery discharge current is less than 380mA. <table> <tr> <th>Control3[8]</th><th>Control7[7]</th><th>IDM Timer</th></tr> <tr> <td>0 (default)</td><td>0 (default)</td><td>40ms (default)</td></tr> <tr> <td>0</td><td>1</td><td>5ms</td></tr> <tr> <td>1</td><td>0</td><td>80ms</td></tr> <tr> <td>1</td><td>1</td><td>1ms</td></tr> </table>	Control3[8]	Control7[7]	IDM Timer	0 (default)	0 (default)	40ms (default)	0	1	5ms	1	0	80ms	1	1	1ms
Control3[8]	Control7[7]	IDM Timer															
0 (default)	0 (default)	40ms (default)															
0	1	5ms															
1	0	80ms															
1	1	1ms															
[6:2]	Not Used	Not Used															
[1]	Battery Only DCProchot# Threshold	Refer to the description of Control0[4:3] in Table 3 .															
[0]	VSYS ABS OV	VSYS absolute overvoltage protection 0 = Enabled (default) 1 = Disabled															

6.4 Information Registers

The Information registers contain SMBus readable information about manufacturing and Operating modes. The following tables identify the bit locations of the available information.

Table 11. Information1 Register 0x3AH

Bit	Description
[3:0]	Not used
[4]	Bit[4] indicates whether the Trickle Charging mode is active. 0 = Trickle Charging mode is not active 1 = Trickle Charging mode is active
[9:5]	Not used
[10]	Bit[10] indicates whether the Low_VSYS_Prochot# is tripped. 0 = Low_VSYS_Prochot# is not tripped 1 = Low_VSYS_Prochot# is tripped
[11]	Bit[11] indicates whether DCProchot# is tripped. 0 = DCProchot# is not tripped 1 = DCProchot# is tripped
[12]	Bit[12] indicates whether ACProchot#/OTGCURRENTProchot# is tripped. 0 = ACProchot#/OTGCURRENTProchot# is not tripped 1 = ACProchot#/OTGCURRENTProchot# is tripped

Table 11. Information1 Register 0x3AH (Cont.)

Bit	Description
[14:13]	Bit[14:13] indicates the active control loop. 00 = MaxSystemVoltage control loop is active 01 = Charging current loop is active 10 = Adapter current limit loop is active 11 = Input voltage loop is active
[15]	Bit[15] indicates whether the internal reference circuit is active. Bit[15] = 0 indicates that the RAA489118 is in Low Power mode. 0 = Reference is not active 1 = Reference is active

Table 12. Information2 Register 0x4DH

Bit	Description
[4:0]	Program Resister read out MaximumSystemVoltage MinimumSystemVoltage Adapter current limit
[7:5]	Bit[7:5] indicates the RAA489118 operation mode. 001 = Boost Mode 010 = Buck Mode 011 = Buck-Boost Mode 101 = OTG Boost Mode 110 = OTG Buck Mode 111 = OTG Buck-Boost Mode
[11:8]	Bit[11:8] indicates the RAA489118 state machine status. 0000 = OFF 0001 = BATTERY 0010 = ADAPTER 0011 = ACOK 0100 = VSYS 0101 = CHARGE 0110 = ENOTG 0111 = OTG 1000 = ENLDO5 1001 = Not Applicable 1010 = TRIM/ENCHREF 1011 = ACHRG 1100 = CAL 1101 = AGON/AGONTG 1110 = WAIT/PSYS 1111 = ADPPSYS
[12]	Bit[12] indicates the BATGONE pin status. 0 = Battery is present (BATGONE low) 1 = No battery (BATGONE high)
[13]	Bit[13] indicates the general purpose comparator output after debounce time. 0 = Comparator output is low 1 = Comparator output is high

Table 12. Information2 Register 0x4DH (Cont.)

Bit	Description
[14]	Bit[14] indicates the ACOK pin status. 0 = No adapter 1 = Adapter is present
[15]	Bit[15] indicates the CONFIG/PSYS state. 0 = CONFIG/PSYS pulled low (NVDC Charging with BFET) 1 = CONFIG/PSYS tied to VDD (Battery charging only with no BFET)

Table 13. Information3 Register 0x90H

Bit	Description
[15:2]	Not used
[1]	Bit[1] indicates the Pass-Through Mode (PTM) status. 0 = PTM is inactive 1 = PTM is active
[0]	Not used