

7. Modulator Information

7.1 RAA489118 Buck-Boost Charger Modes of Operation

The RAA489118 buck-boost charger drives an external N-channel MOSFET bridge made of two transistor pairs as shown in Figure 38. The first pair, Q1 and Q2, is a buck arrangement with the transistor center tap connected to an inductor input as is the case with a buck converter. The second transistor pair, Q3 and Q4, is a boost arrangement with the transistor center tap connected to the output of the inductor as is the case with a boost converter. This arrangement supports bucking from a voltage input higher than the battery and also boosting from a voltage input lower than the battery.

Table 14. Operation Mode

Mode	Q1	Q2	Q3	Q4
Buck	Control FET	Sync. FET	OFF	ON
Boost	ON	OFF	Control FET	Sync. FET
Buck-Boost	Control FET	Sync. FET	Control FET	Sync. FET
OTG Buck	ON	OFF	Sync. FET	Control FET
OTG Boost	Sync. FET	Control FET	OFF	ON
OTG Buck-Boost	Sync. FET	Control FET	Sync. FET	Control FET
Pass-Through	ON	OFF	OFF	ON

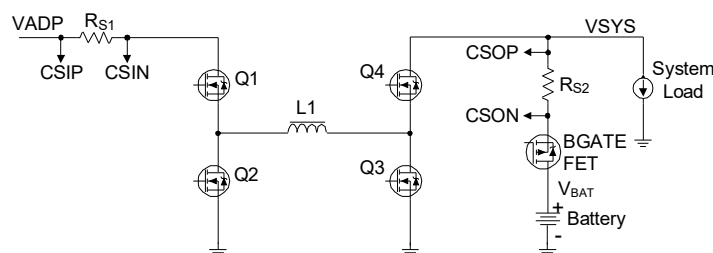


Figure 38. Buck-Boost Charger Topology

The RAA489118 optimizes the Operation mode transition algorithm by comparing the input and output voltage ratio and the load condition. When the adapter voltage V_{ADP} is rising and is higher than 91% of the system bus voltage $VSYS$, the RAA489118 transitions from Boost mode to Buck-Boost mode. If V_{ADP} is higher than 114% of $VSYS$, the RAA489118 forcedly transitions from Buck-Boost mode to Buck mode. At heavier loads, the mode transition point changes accordingly to accommodate the duty cycle change due to the power loss on the charger circuit.

When the adapter voltage V_{ADP} is falling and is lower than 108% of the system bus voltage $VSYS$, the RAA489118 transitions from Buck mode to Buck-Boost mode. If V_{ADP} is lower than 85% of $VSYS$, the RAA489118 transitions from Buck-Boost mode to Boost mode.

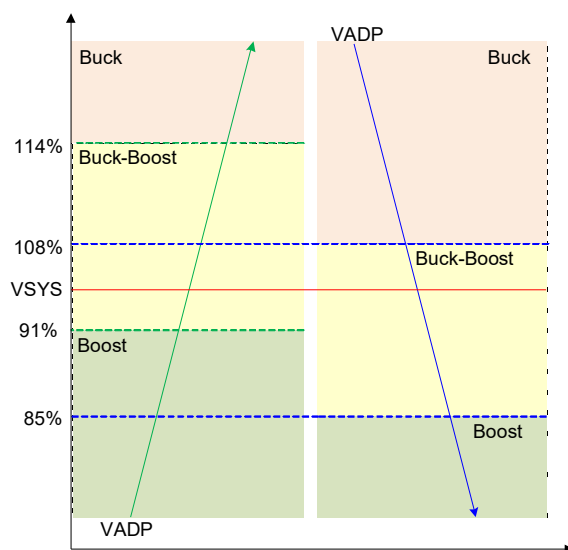


Figure 39. Operation Mode

When the Force Buck Mode is enabled by setting the Control0 Bit[1] to 1, the RAA489118 operates in Buck mode instead of Buck-Boost mode when VADP is 480mV higher than VSYS. Force Buck mode has a 240mV hysteresis window, so the RAA489118 operates in Buck-Boost mode when VADP is lower than VSYS + 240mV.

7.2 USB On-the-Go (USB OTG)

When the On-the-Go (OTG) function is enabled with the SMBus command and OTGEN pin, and if the battery voltage V_{BAT} is higher than 4.5V, the RAA489118 operates in OTG mode and Control2 Bit[5] controls ASGATE. BATGONE must be low to enable OTG mode.

When the OTG function is enabled with the SMBus command and OTGEN pin and if the battery voltage V_{BAT} is higher than 4.5V, the RAA489118 operates in Reverse Buck, Reverse Boost, or Reverse Buck-Boost mode.

When the RAA489118 receives the command to enable the OTG function, it starts switching after the debounce time set by Control2 register Bit[13] and Control3 register Bit[0]. When the OTG output voltage reaches the OTG output voltage set by register 0x49 Bit[14:3], OTG power-good OTGPG asserts to high. Control2 register Bit[5] can also be used to turn the ASGATE FET off to cut off the OTG output.

Before OTG mode starts switching, the CSIP pin voltage needs to drop below the OTG output overvoltage protection threshold (OTG Voltage DAC(0x49h) + 1.8V) first. The CSIP pin is the output sensing point in OTG mode.

The default OTG output voltage is 5.004V. The OTG Voltage register 0x49h configure the OTG output voltage.

The default OTG output current is 512mA when R_{S1} is 10mΩ. The OTG Current register 0x4Ah can be used to adjust the OTG output current limit.

The RAA489118 includes the OTG output undervoltage and overvoltage protection functions. The UVP threshold is OTG output voltage -1.8V and the OVP threshold is OTG output voltage +1.8V.

When UV is detected, the RAA489118 de-asserts OTGPG. After 32ms, it stops switching and turns off ASGATE. It resumes switching after the debounce time set by Control2 register Bit[13] and Control3 register Bit[0].

When OV is detected, the RAA489118 de-asserts OTGPG. It resumes switching when the OTG voltage drops below the OTG Voltage DAC value specified at 0x49.

BATGONE must be low to enable OTG mode.

7.3 Pass-Through Mode

Pass-Through Mode (PTM) is configured by Control2 register Bits[1:0]. When PTM (normal or forced) is enabled, the internal reference for the output voltage ramps to the input voltage, and switching continues until the output voltage is within $\pm 150\text{mV}$ of the input (adapter) voltage. Once the output voltage falls within this 300mV window, switching stops, Q1 and Q4 are set on, and Q2 and Q3 are turned off. When PTM is enabled, all protections are still active.

To disable PTM, set Control2 register Bits[1:0] = 00. On exiting PTM, the internal reference for the output voltage ramps to the MaximumSystemVoltage DAC value, and switching resumes. Normal PTM is also exited if any of the following criteria are encountered:

- Adapter OV triggers
- Ideal Diode Mode is entered
- The battery discharge current exceeds 600mA (for $R_{S2} = 5\text{m}\Omega$)
- VSYS absolute OV triggers

Forced PTM can only be exited by disabling PTM using Control2 Bits[1:0].

Before entering Pass-Through mode, the following is recommended:

1. Ensure CV mode operation;
2. Enable slew rate limiting by setting Control6 Bit[6] = 1; and
3. Change the MaximumSystemVoltage DAC to a value as close to the V_{ADP} voltage as possible.

When Q1 and Q4 are latching on to enter Pass-Through mode, the adapter current limit loop turns on for more than 1ms .

7.4 Modulator Control Loops

Figure 40 shows the modulator's four main control loops. Each loop has a DAC register to provide settings as needed for each system.

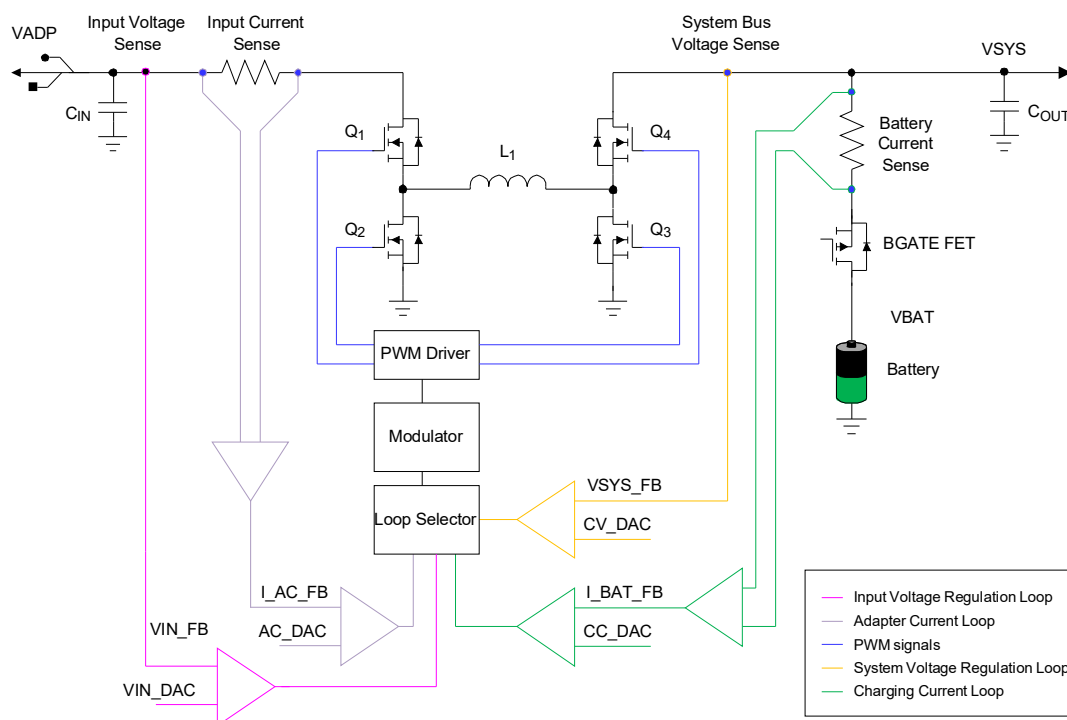


Figure 40. Charger Control Loops

7.4.1 Adapter Current Loop and Two-Level Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command to register address 0x3FH and, optionally, an AdapterCurrentLimit2 command to register address 0x3BH using the Write-word protocol. See [Table 2](#) for the DAC summary of values.

The RAA489118 limits the adapter current by limiting the CSIP - CSIN voltage. By using the recommended R_{S1} current sense resistor of 10m Ω , the LSB of the register translates to 8mA of adapter current.

After adapter POR, the AdapterCurrentLimit1 register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit2 register is set to its default value of 1.504A or keeps the value that is written to it previously if the battery is present first. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their content. By default, the two level adapter current limit is disabled.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register.

The two-level adapter current limit function can be enabled and disabled through SMBus Control2 register Bit[12] and the t1, t2 settings are configured by the Control5 register. When the two-level adapter current limit function is disabled, only the AdapterCurrentLimit1 value is used as the adapter current limit and AdapterCurrentLimit2 value is ignored.

In a real system, a Turbo event usually does not last very long. It is often no longer than milliseconds, a time length during which the adapter can supply current higher than its DC rating. The RAA489118 uses a two-level adapter current limit to fully take advantage of the surge capability of the adapter and minimize the power drawn from the battery.

[Figure 41](#) shows the two SMBus programmable adapter current limit levels, AdapterCurrentLimit1 and AdapterCurrentLimit2, as well as the durations t1 and t2. The two-level adapter current limit function is initiated when the adapter current is less than 100mA lower than the AdapterCurrentLimit1 register setting. It starts at AdapterCurrentLimit2 for duration t2, then changes to AdapterCurrentLimit1 for duration t1 before repeating the pattern. These parameters can set the adapter current limit with an envelope that allows the adapter to temporarily output surge current without requiring the charger to enter Turbo mode. This operation maximizes battery life.

The AdapterCurrentLimit1 register value can be higher or lower than the AdapterCurrentLimit2 value.

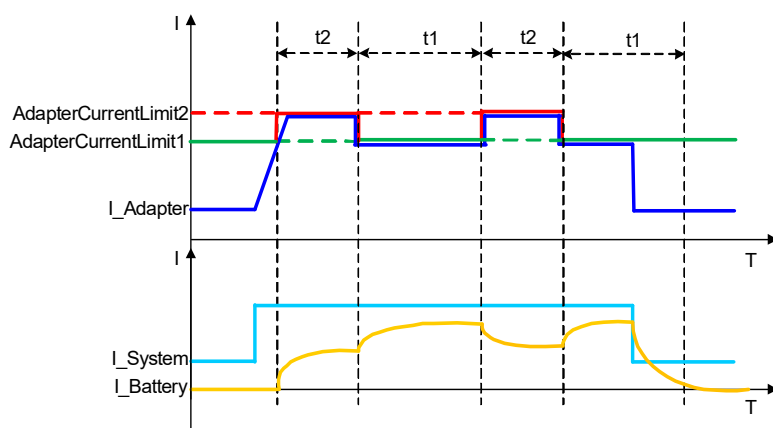


Figure 41. Two-Level Adapter Current Limit

7.4.2 USB-PD On-the-Go Output Current

The OTG output current regulation register DAC (Table 2) contains the SMBus readable and writable current that the current sense loop tries to regulate. This loop reuses the input current sense amplifier. If you are using the USB-PD Programmable Power Supply, this is the current limit loop. *Note:* Renesas recommends disabling OTG undervoltage protection when OTG current limiting mode is anticipated as part of normal operation.

7.4.3 Input Voltage Regulation Loop

7.4.3.1 Adapter Minimum Voltage

The input voltage regulation register DAC (Table 2) contains the SMBus readable and writable input voltage limit at which the input voltage loop tries to regulate when the input voltage is dropping. When the ADP is browning out or weak, the input voltage can droop and the input voltage loop tries to regulate to this setting by reducing battery charging current and then system power to try to hold up the input voltage. The system voltage might start to drop if the input power is not high enough to support the system.

7.4.3.2 USB-PD On-the-Go Minimum Battery Voltage

The input voltage regulation register DAC (Table 2) sets a minimum voltage for VBAT when operating in OTG mode. Control5 register Bit[11] enables and disables the battery voltage (VBAT) regulation loop. This regulation loop can be used to prevent over-discharging of a battery when operating in OTG mode (for example, USB-PD source mode).

7.4.4 USB-PD On-the-Go Output Voltage

The OTG output voltage regulation register DAC (Table 2) contains the SMBus readable and writable voltage that the voltage loop tries to regulate. This loop reuses the input voltage sense amp.

This register accepts any voltage value, but only the valid register bits are written to the register. The maximum value is clamped.

7.4.5 System Voltage Regulation and Trickle Charging

This loop works with two different voltage settings, MaxSystemVoltage and MinSystemVoltage.

The MaxSystemVoltage register sets the battery full charging voltage limit. In NVDC charging mode, the MaximumSystemVoltage register setting is also the system bus voltage regulation point when the battery is absent or when the battery is present but not in Charging mode.

The VSYS pin senses the battery voltage for maximum charging voltage regulation. The VSYS pin is also the system bus voltage regulation sense point.

If the battery is absent, the BGATE is turned off (no charging) and the system voltage is regulated to the same setting as the MaxSystemVoltage DAC(0x15h). To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command to register address 0x15H using the Write-word protocol shown in Figure 37.

The RAA489118 supports trickle charging to overly discharged batteries. It can activate the trickle charging function when the battery voltage is lower than MinSystemVoltage setting. The VBAT pin is the battery voltage sense point for Trickle Charge mode.

To enable Trickle Charging, set the ChargeCurrent register to a non-zero value. To disable trickle charging, set the ChargeCurrent register to 0. See Table 15 for trickle charging control logic.

The trickle charging current can be programmed to be 1024mA, 512mA, 256mA, or 128mA (with 5mΩ R_{s2}) through SMBus Control2 register Bit[15:14] as shown in Table 5.

In Trickle Charging mode, the RAA489118 regulates the trickle charging current through the buck-boost switcher. Provided that a BFET is present, another independent control loop drives the BFET gate so that the system voltage is maintained at the voltage set in the MinSystemVoltage register. If there is no BFET, the system voltage

might fall below the MinSystemVoltage setting. The VSYS pin is the system voltage sensing point in Trickle Charging mode.

When the battery voltage is charged to the MinSystemVoltage register value, the RAA489118 enters Fast Charging mode by limiting the charging current at the ChargeCurrentLimit register setting, which is typically higher than the trickle charge current.

7.4.6 Charging Current Loop

This loop uses the charge current DAC (see [Table 2](#)) to set the fast charging current limit. To set it, write a 16-bit ChargeCurrentLimit command to register address 0x14H ([Table 1](#)).

The RAA489118 limits the charging current by limiting the CSOP - CSON voltage. Therefore, the charge current depends on the R_{s2} resistor value. For example, if the current sense resistor R_{s2} is halved, the regulated charge current doubles. By using the current sense resistor $R_{s2} = 5m\Omega$, the LSB of the register translates to 8mA of charging current. The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register.

7.4.6.1 Reverse Mode Discharge Current

When the charger is in reverse mode of operation (OTG), there is a discharge current limit loop that is set by 2x the Charge Current limit register (0x14). This discharge current limit loop is in addition to the voltage regulation loop set by the OTG Voltage register, the current limit loop set by the OTG Current register, and the optional VBAT regulation loop set by the Input Voltage register. The discharge current limit loop is disabled when charge current limit (0x14h) is zero. When the charge current is a non-zero value, the charger limits the battery discharge current to be less than the discharge current limit (2x the Charge Current limit). This function can be used to limit inrush current from the battery when the OTG Voltage ramps up or down (in addition to the slew rate function).

7.4.7 Turbo Mode Support

Turbo mode refers to the system drawing more power than the power rating of the adapter.

If the adapter current reaches the AdapterCurrentLimit1 register set value (or the AdapterCurrentLimit2 register set value, if the two-level adapter current limit function is enabled), or the adapter input voltage drops to the Input Voltage Regulation Reference set by Input Voltage DAC register (0x4B), the RAA489118 limits the input power by regulating the adapter current at the AdapterCurrentLimit1/2 register set value, or by regulating the adapter voltage at the Input Voltage Regulation Reference point.

In Turbo mode, the system bus voltage VSYS drops automatically or the charging current drops automatically to limit the adapter input power. If the VSYS pin voltage is 150mV lower than the VBAT pin voltage, the BGATE FET turns on so that the battery supplies the rest of the power required by the system.

If the RAA489118 detects 250mA charging current or if the battery discharging current is less than 380mA for longer than the IDM exit timeout (80ms, 40ms, 5ms, or 1 ms), BGATE turns off and Turbo mode exits. The Turbo mode exit timer is configured through Control3 register 0x4C Bit[8] and Control7 register 0x36 Bit[7]. See [Table 15](#) for BGATE control logic.

Table 15. BGATE On/Off Truth Table

Turbo (Control Bit)	ChargeCurrent Register	BGATE On/Off	
		System Load Not In Turbo Mode Range	System Load in Turbo Mode Range
0 = Enable 1 = Disable	0 = Zero 1 = Nonzero		
0	0	OFF	ON
0	1	ON for fast charge; Trickle charge is enabled	ON
1	0	OFF	OFF
1	1	ON for fast charge; Trickle charge is enabled	ON

7.5 R3 Modulator

The RAA489118 uses the patented Renesas Robust Ripple Regulator (R3) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. [Figure 42](#) conceptually shows the R3 modulator circuit, and [Figure 43](#) shows the operation principles in steady state.

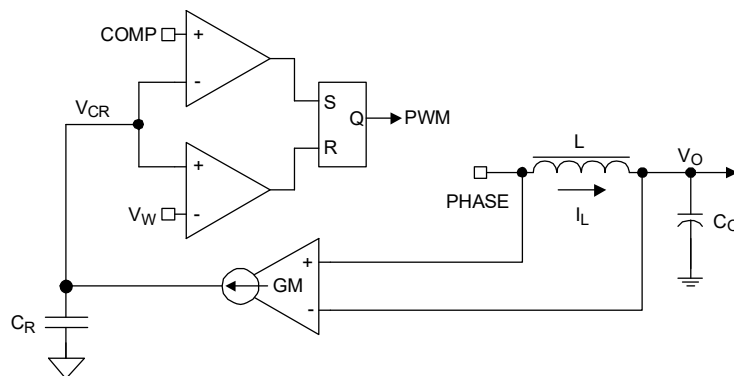


Figure 42. R3 Modulator

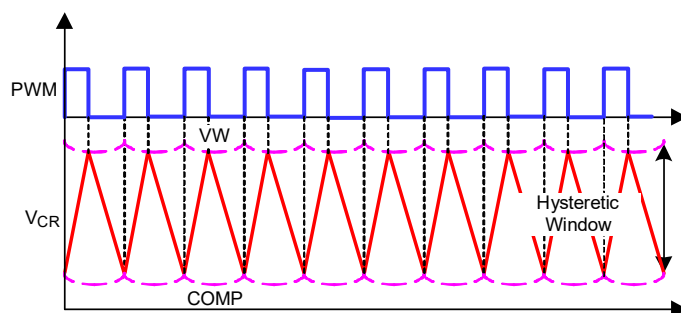


Figure 43. R3 Modulator Operation Principles In Steady State

A fixed voltage window (VW window) exists between VW and COMP. The modulator charges the ripple capacitor C_R with a current source equal to $g_m(V_{IN}-V_O)$ during PWM on-time and discharges the ripple capacitor C_R with a current source equal to $g_m V_O$ during PWM off-time, where g_m is a gain factor. The C_R voltage V_{CR} therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{CR} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{CR} , which is large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulator.

Figure 44 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, turning on PWM pulses earlier and more frequently temporarily, which allows for higher control loop bandwidth than conventional fixed frequency PWM modulators at the same steady state switching frequency.

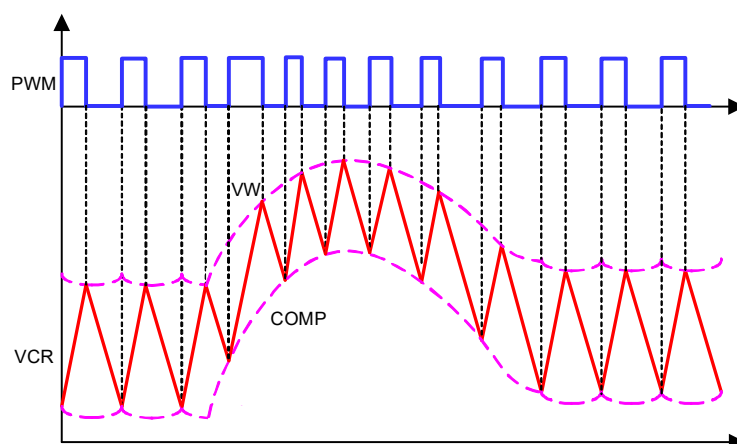


Figure 44. R3 Modulator Operation Principles In Dynamic Response

The R3 modulator can operate in Diode Emulation (DE) mode to increase light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, which emulates a diode. As shown in [Figure 45](#), when LGATE is on, the low-side MOSFET carries current and creates negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

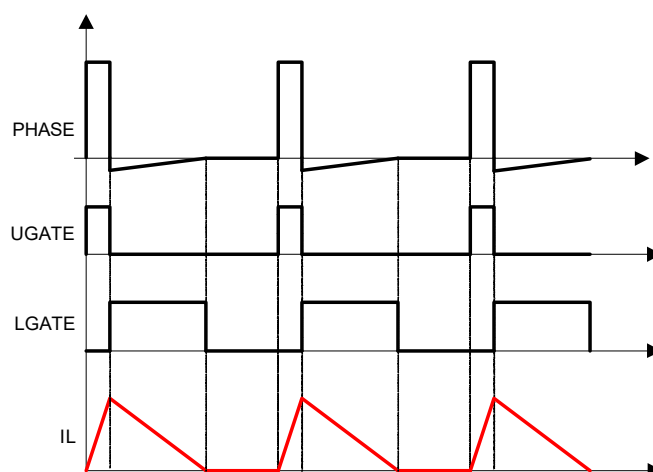


Figure 45. Diode Emulation

If the load current is light enough, as [Figure 45](#) shows, the inductor current reaches and stays at zero before the next phase node pulse, and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A, and the regulator is in Continuous Conduction Mode (CCM) although the controller is in DE mode.

[Figure 46](#) shows the operation principle in DE mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore is the same, so the inductor current triangle is the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{CR} in DE mode to mimic the inductor current. The COMP voltage takes longer to reach V_{CR} , which naturally stretches the switching period. The inductor current triangles move farther apart from each other so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.